WHAT IS CLAIMED IS:

1. A method for controlling a voltage controlled oscillator (VCO) in a bang-bang phase-locked loop, the method comprising:

changing a VCO frequency by a first step size upon establishing frequency lock; and

changing the VCO frequency by a second step size some time after the VCO frequency has been changed by the first step size;

wherein the first step size is larger than the second step size.

2. The method of claim 1 wherein said first step size provides a faster VCO frequency pull-in rate than the second step size.

3. The method of claim 1 additionally comprising limiting the time during which the VCO frequency is changed by the first step size.

4. The method of claim 1 additionally comprising transitioning from changing the VCO frequency by the first step size to changing the VCO frequency by the second step size through at least one intermediate step size intermediate between said first and second step sizes.

5. The method of claim 4 wherein said transitioning includes low pass filtering an analog step size signal.

6. The method of claim 4 wherein said transitioning includes changing a counter value and setting the step size in response to the counter value.

7. The method of claim 4 wherein said transitioning includes changing a counter value up or down in response to a comparison of the counter value with a programming input.

8. The method of claim 1 including transitioning from the first step size to the second step size in response to a control signal that indicates frequency lock.

9. The method of claim 8 wherein the transitioning includes generating a delayed response to the control signal that indicates frequency lock.

10. The method of claim 1 further including programming the first and second step sizes.

11. A system for controlling a voltage controlled oscillator (VCO) in a bang-bang phase-locked loop, the system comprising:

a step size controller configured to:

provide a first VCO control signal to the VCO upon establishing frequency lock, said first VCO control signal causing the VCO frequency to change by a first step size; and

provide a second VCO control signal to the VCO some time after the VCO frequency has changed in response to the first VCO control signal, said second VCO control signal causing the VCO frequency to change by a second step size, wherein the first step size is larger than the second step size.

12. The system of claim 11 wherein the step size controller is configured to limit the time over which the VCO frequency is changed by the first step size.

13. The system of claim 11 wherein the step size controller is additionally configured to transition from providing the first VCO control signal to providing the second VCO control signal by providing at least one intermediate VCO control signal, said at least one intermediate VCO control signal causing the VCO frequency to change by a step size intermediate between said first and second step sizes.

14. The system of claim 11 wherein the step size controller is configured to transition to providing the second VCO control signal in response to a control signal that indicates frequency lock.

15. The system of claim 11 wherein the step size controller comprises:

timing control logic configured to control the timing of transitioning from the first VCO control signal to the second VCO control signal in response to a control signal that indicates frequency lock; and

step size logic in signal communication with the timing control logic configured to transition from the first VCO control signal to the second VCO control signal in response to a timing control signal from the timing control logic.

16. A system for controlling a voltage controlled oscillator (VCO) in a bang-bang phase-locked loop, the system comprising:

timing control logic configured to control the timing of changes in VCO frequency step size in response to a control signal that indicates frequency lock; and

step size logic in signal communication with the timing control logic configured to change the VCO frequency step size from a first step size to a second step size in response to a timing control signal from the timing control logic, wherein the first step size is larger than the second step size.

17. The system of claim 16 wherein the timing control logic includes delay logic for generating the timing control signal by delaying the control signal that indicates frequency lock.

18. The system of claim 16 wherein the step size logic includes a digital-to-analog converter for converting digital step size signals into an analog step size signal.

19. The system of claim 16 wherein the step size logic is configured to output a step size signal to the VCO, which sets the VCO frequency step size.

20. The system of claim 16 wherein the step size logic includes an up/down counter and a comparator, the comparator being configured to compare a counter value from the counter with a programming input and to output a signal that causes the up/down counter to increment or decrement in response to the comparison.

21. The system of claim 16 wherein the step size logic includes a programming input for receiving step size information.